POST CMOS PATHFINDING

Leti Innovation Days | June 28-29, 2017

DEVELOPING THE BUILDING BLOCKS FOR DATA PROCESSING

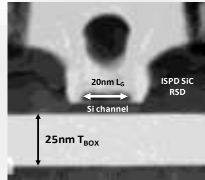
- **The challenges to continue the performance improvement of data processing systems are multiple**
  - Improve the energy efficiency to maintain at least constant the overall dissipation while continuing the exponential increase in computational power
  - Reduce the bottleneck in the memory-processing communication
  - Increase the density of the functions while reaching the limits of scaling

- **In LETI we are addressing these issues with a number of technological developments**
  - Efficient use of new devices
  - 3D integration at different granularities
  - New computing architectures

DEVELOPING THE BUILDING BLOCKS FOR DATA PROCESSING

Power efficient FDSOI

22FD



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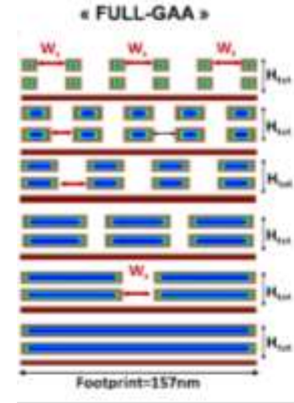
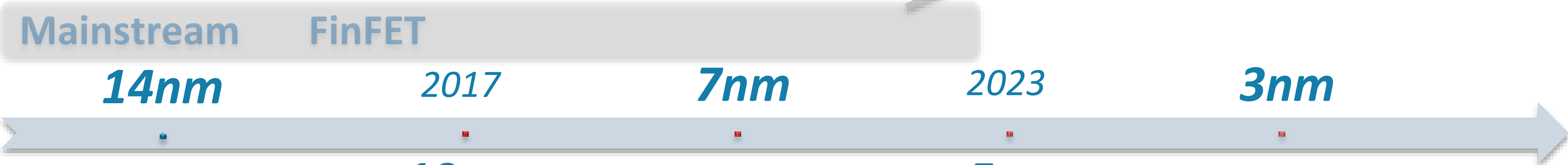
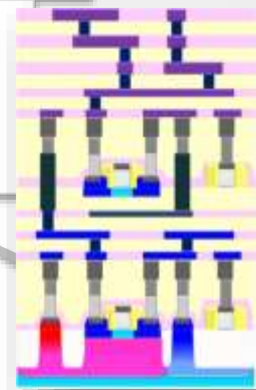


Non planar / Stacked NW



Disruptive scaling

Alternative to scaling and diversification



Hybrid logic

Mechanical switches

Cryo CMOS

Si Quantum bits

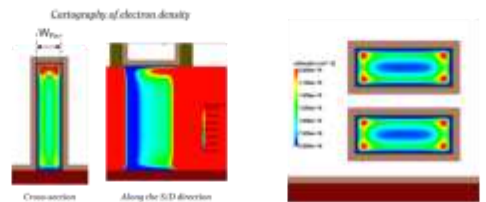
CoolCube^{TM} for 3D VLSI

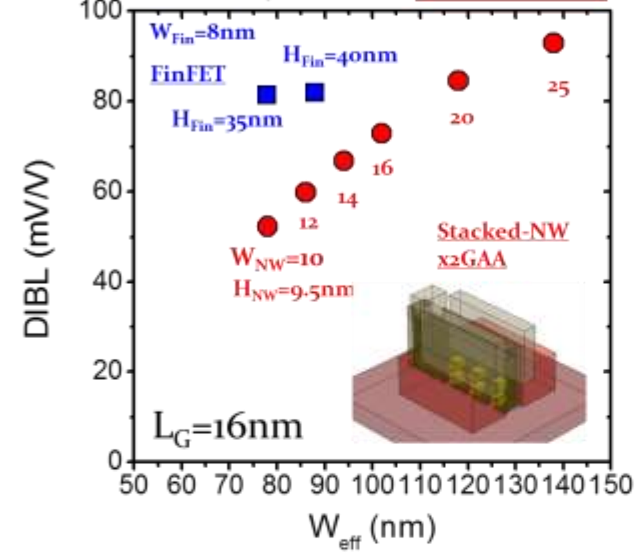
Early design coupling

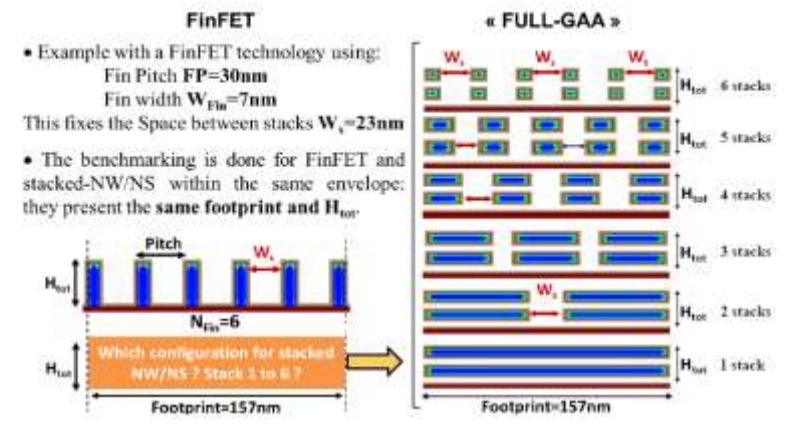
STACKED NANOWIRES FOR 7NM AND BEYOND

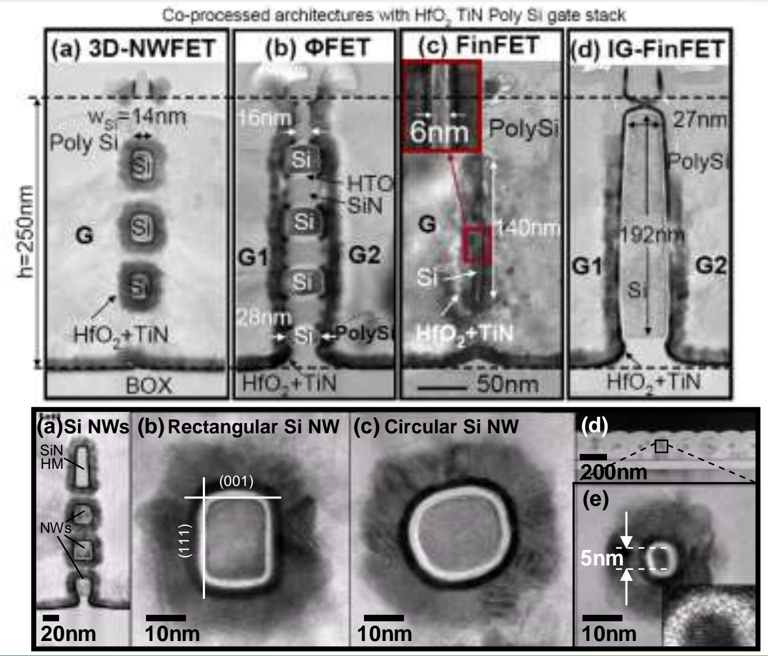
Technological challenges

- *Strain implementation*
- *Access resistance (material, aspect ratio)*
- *Parasitic capacitances decrease*
- *Selective removal (SiGe vs Si/Si vs SiGe)*
- *Surface roughness control and multiVt platform*

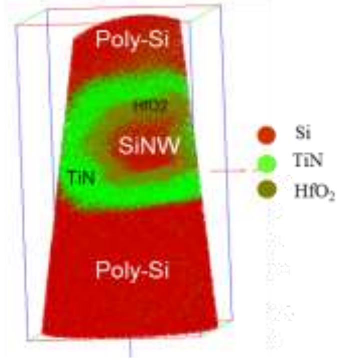




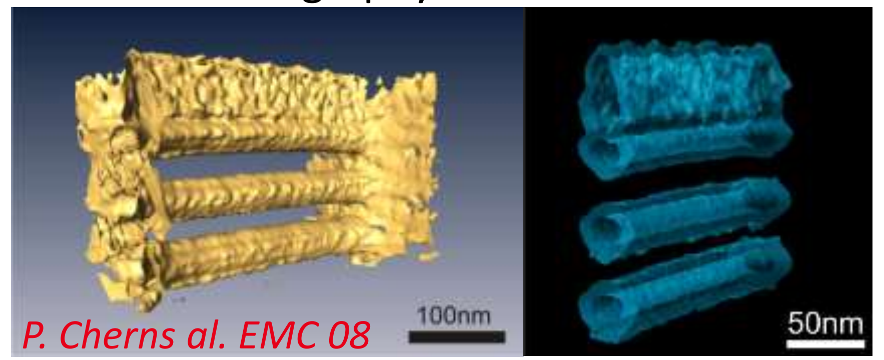




Atom probe tomography



Electron tomography

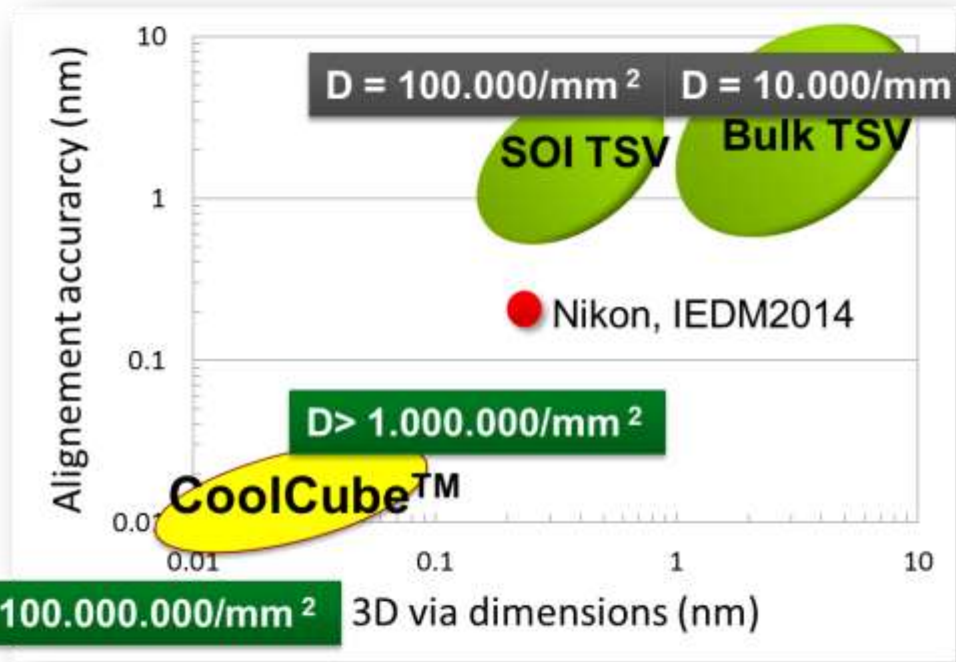


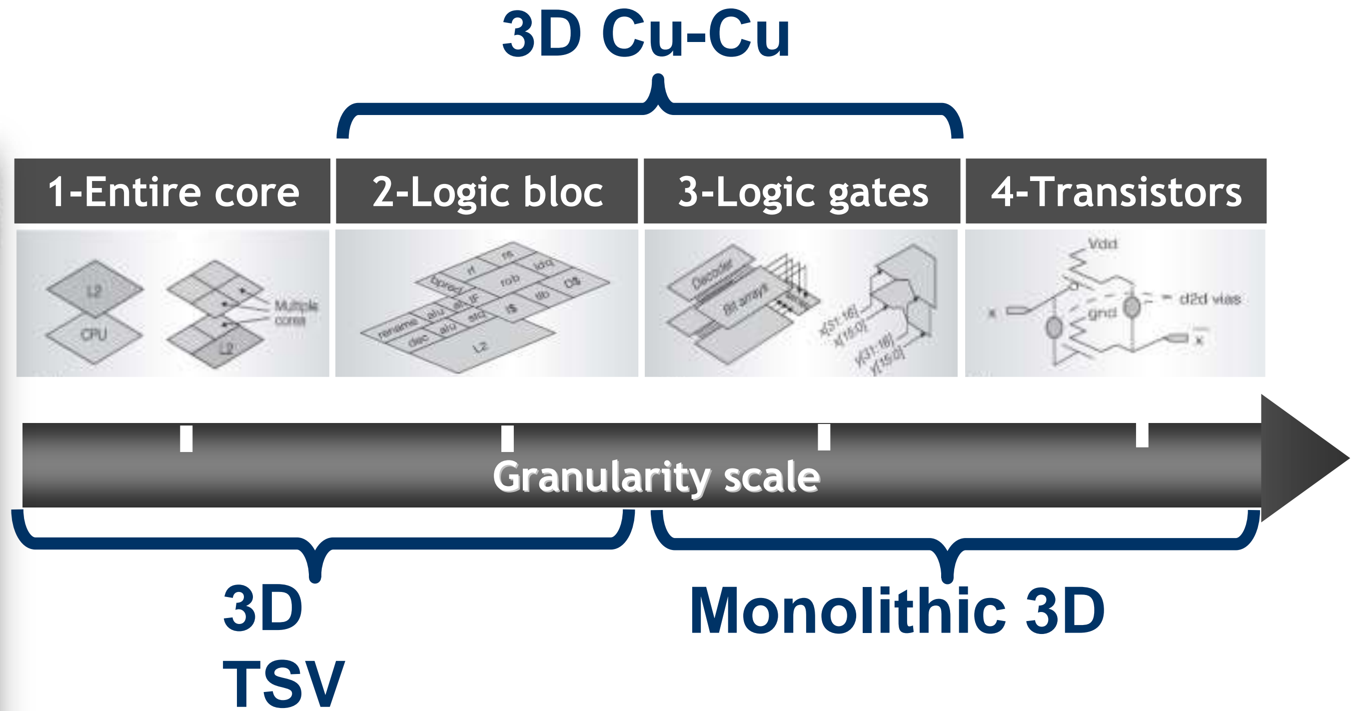
P. Cherns al. EMC 08

T. Ernst IEDM 2006, C. Dupré IEDM 2008, E. Bernard IEEE EDL 2009, S. Barraud IEDM 2016

OUR VIEW TODAY FOR COMPUTING

3D FOR DESIGN OPTIMISATION





→ Gain obtained by shortening interconnection, optimising function and cost by partitioning and reducing latency

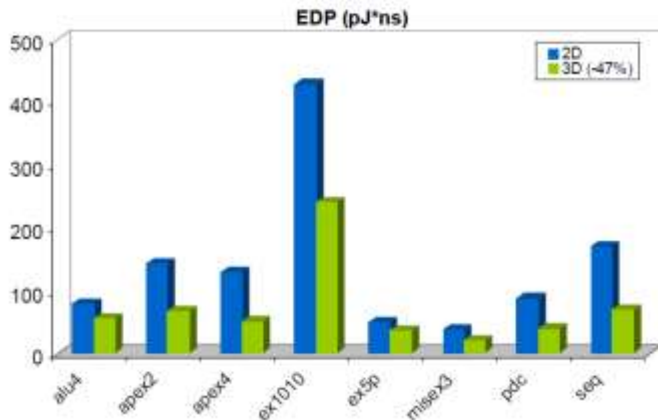
COOLCUBE™

- *Further density scaling*
- *Cost optimization*
- *Added functionnality*

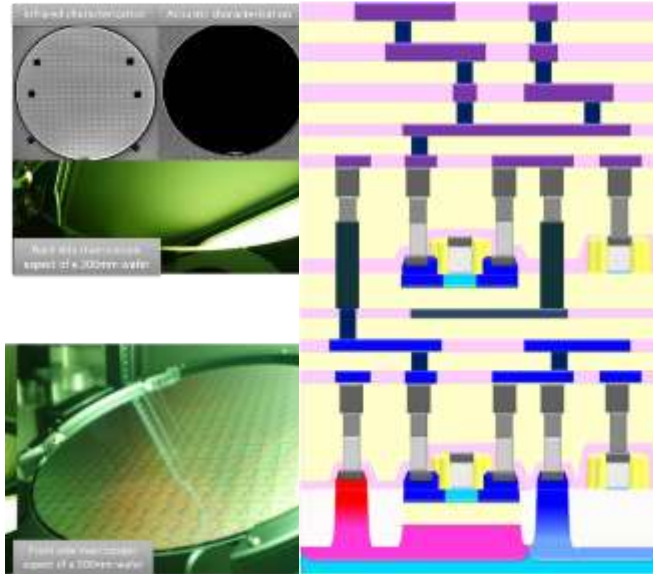
Design tools and 2D vs 3D benchmark

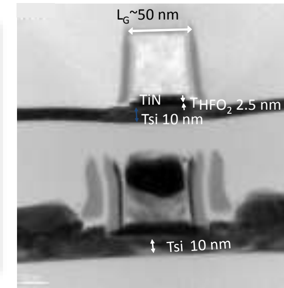
Average gain benchmark 2D vs 3D

- Area gain=55%
- Perf gain = 23%
- Power gain = 12%

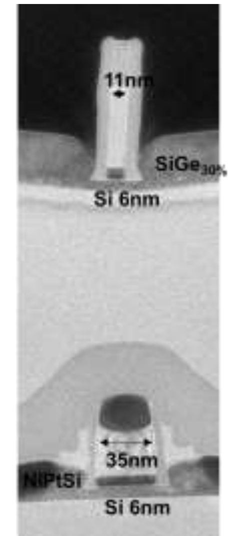


Energy-delay product of FPGA benchmark circuits for 2D and 3D architectures

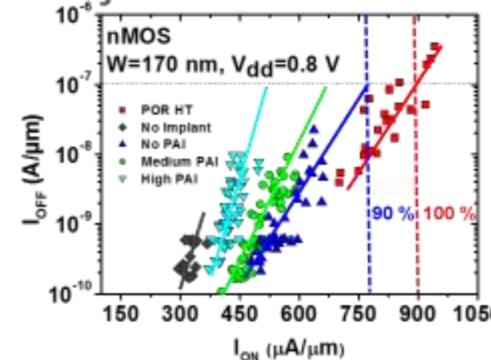


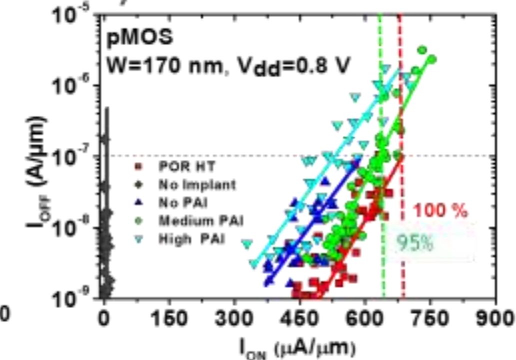


III-V on top of SiGe, with IBM-Zurich - VLSI 2017



Objective: the same as bottom layer





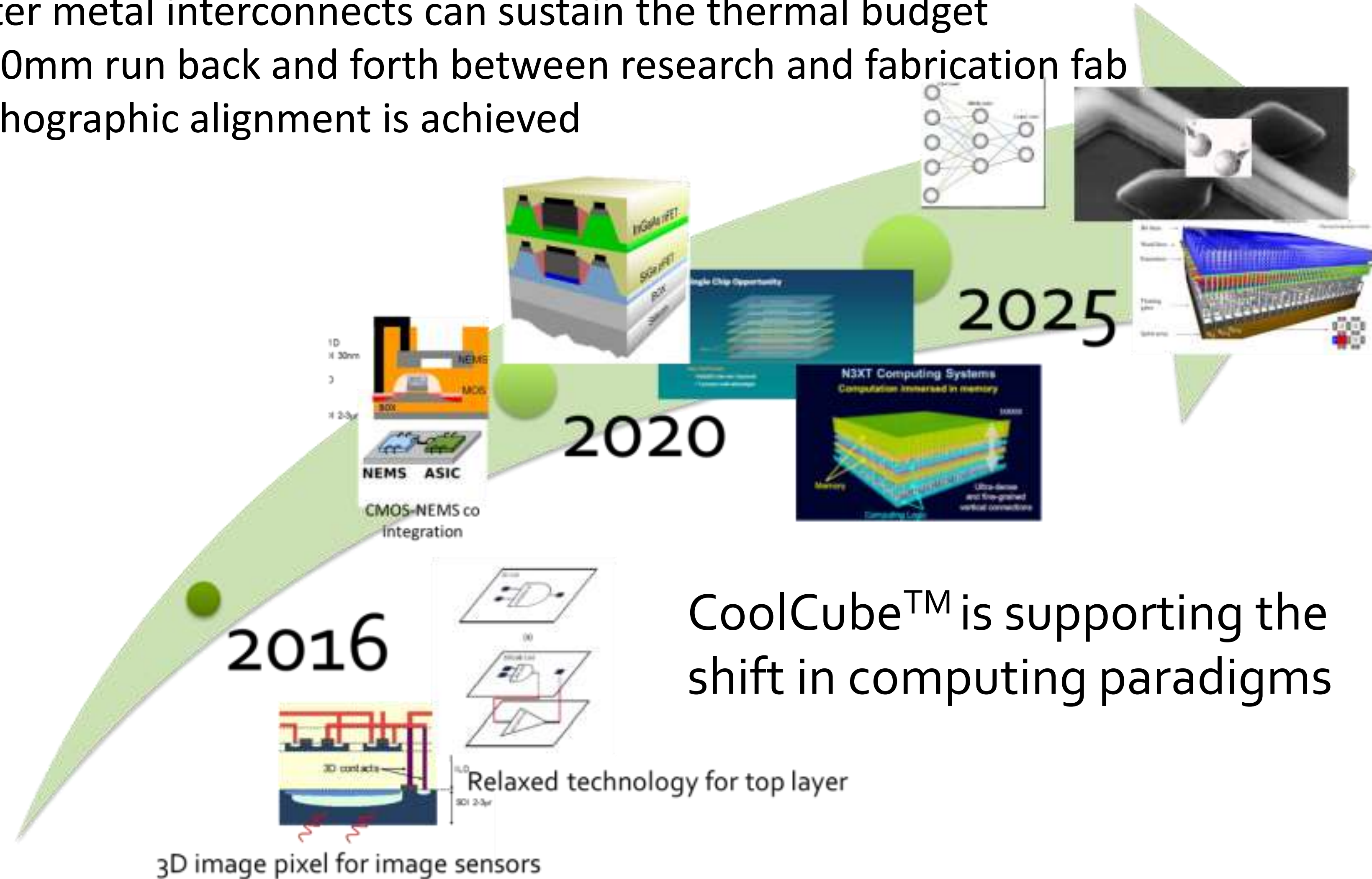
14 FDSOI low thermal budget electrical characteristics

- **Module developments**
- **Full 300mm integration route**
- **Compact modeling, DRM, PDK**
- **IC design**

P Batude, IEDM'09, P Batude, IEDM'11, L Pasini, IWJT '14, P Batude, IITC '14, C Fenouillet-Beranger, IEDM '14, P Batude, VLSI'15, L. Pasini, VLSI'15 & '16, L Brunet, VLSI '16

Future of 3D developments

- ✓ Top layer performance has been demonstrated
- ✓ Inter metal interconnects can sustain the thermal budget
- ✓ 300mm run back and forth between research and fabrication fab
- ✓ Lithographic alignment is achieved



CoolCube™ is supporting the shift in computing paradigms

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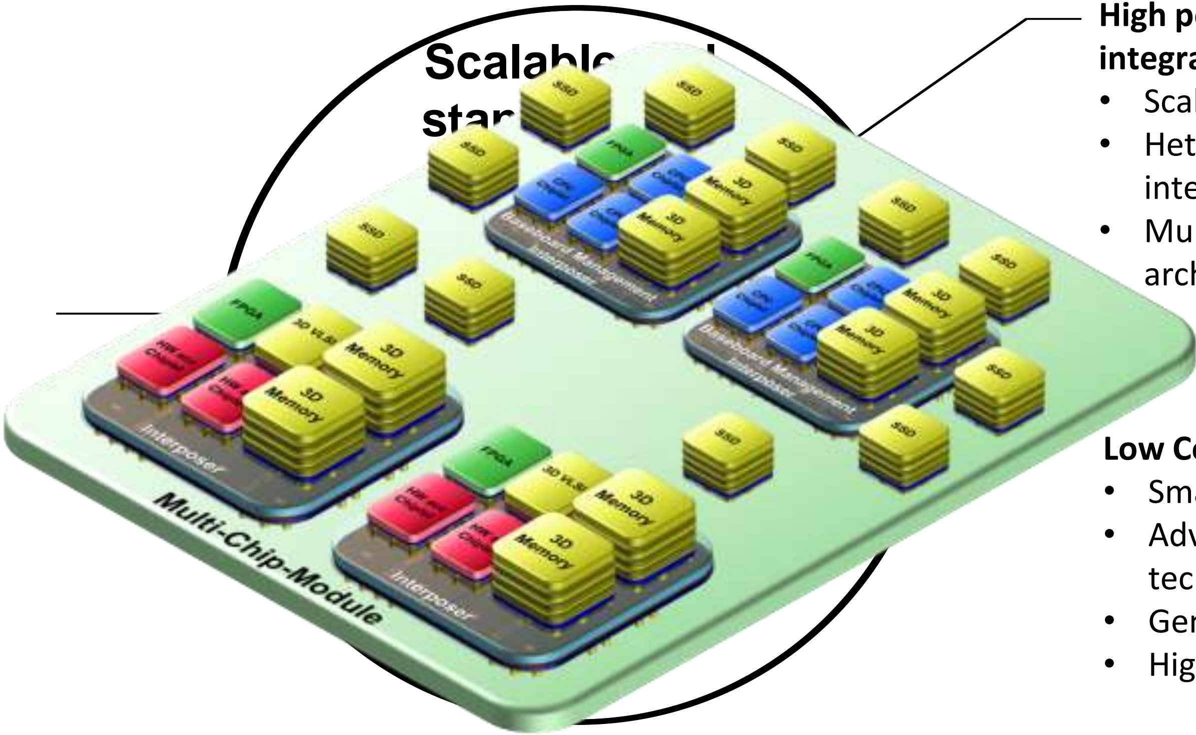
OUR VIEW TODAY TO SCALE UP COMPUTING

Chiplets On Interposer

Specialisation in the interposer:

- System-in-Package, Silicon (Passive or active), photonic
- Application dependent



High performance integration:

- Scale-out
- Heterogeneous integration
- Multicore architectures

Low Cost Chiplet

- Small chips
- Advanced technology
- Generic
- High volume

NEW ARCHITECTURES DEVELOPMENT: NEURAL NETWORK DESIGN

N2D2

Learning and Test DB

Data conditioning

Modeling

Learning

Optimization

Eval.

Program.

Synthesis

Learning toolbox

Application constraints

Integration constraints

Emulated NN: MPSOC, DSP, GPU, FPGA

Digital IC: PNeuro, Spike NN

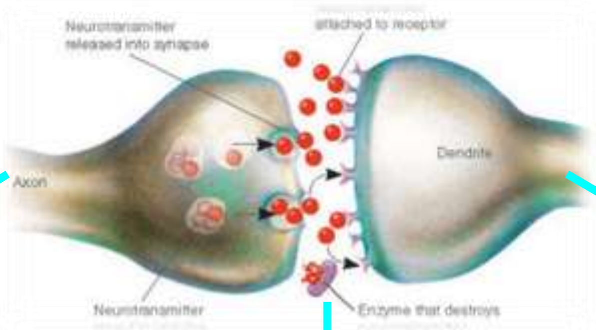
Mix Signal IC: Spider, Reptile, NVRAM + Spike

Energy Efficiency

Technology Accessibility

(Credit: *maxsattana / Fotolia*)

NEW TECHNOLOGIES FOR NEW ARCHITECTURES: RRAM AS SYNAPSES



Thermal effect

PCM

GST
GeTe
GST + HfO_2

M.Suri, et. al, IEDM 2011
M.Suri, et. al, IMW 2012 , JAP 2012
O.Bichler et al. IEEE TED 2012
M.Suri et al., EPCOS 2013
D.Garbin et al., IEEE Nano 2013

Electronic effect oxygen vacancies

OXRAM

TiN/HfO_2/Ti/TiN

D.Garbin et al. IEDM 2014
D.Garbin et al., IEEE TED 2015

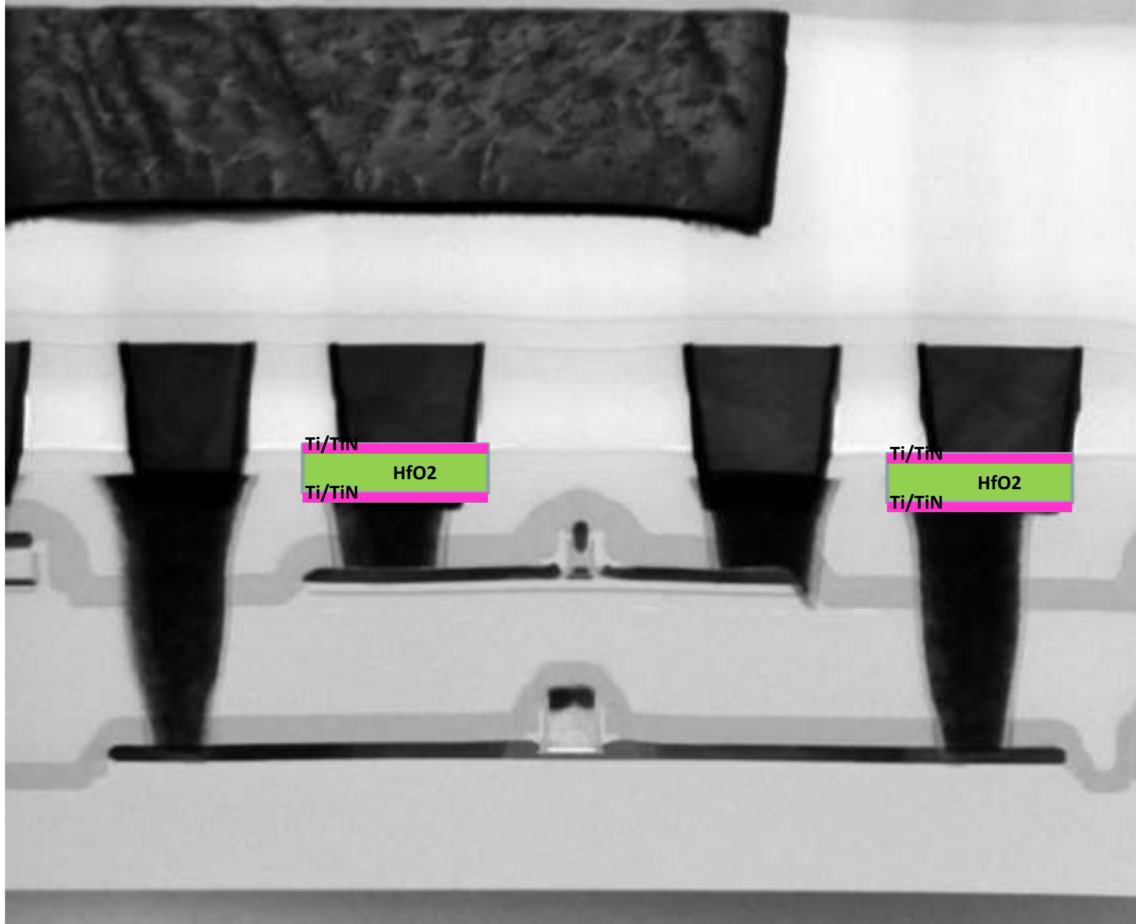
Electrochemical effect

CBRAM

Ag / GeS_2

M.Suri et al., IEDM 2012
M.Suri et al., IEEE TED 2013

3D INTEGRATION COUPLED WITH RRAM



Short term structure

- → **RRAM on top level to avoid contamination issue**
- → **Reuse of existing masks plus ebeam to build 1T1R**

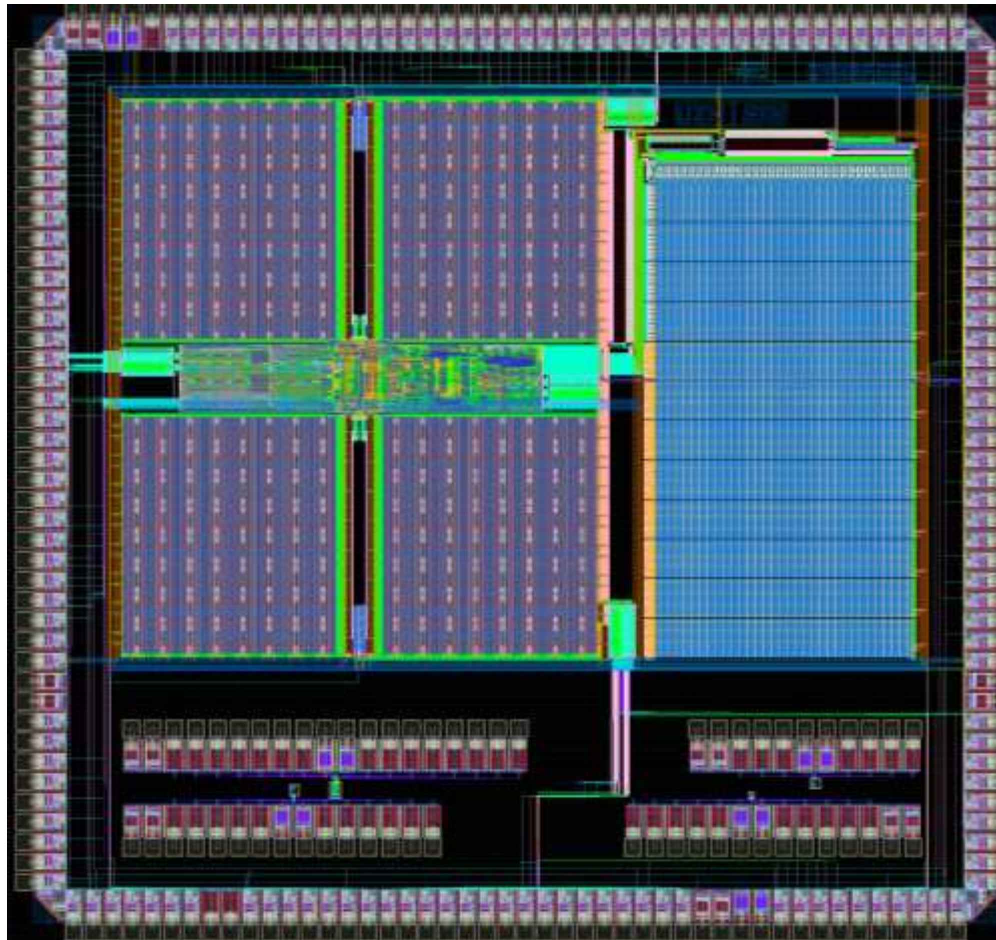
No W or Cu between the 2 levels → avoid contamination in first trial

1 base ebeam required for RRAM definition
RRAM based on HfO_2/Ti/TiN low temp materials (~ 350°C) → no critical problems to integrate on the top level

MULTICORE SPIKING NEUROMORPHIC PROCESSOR IN FDSOI 28NM CMOS

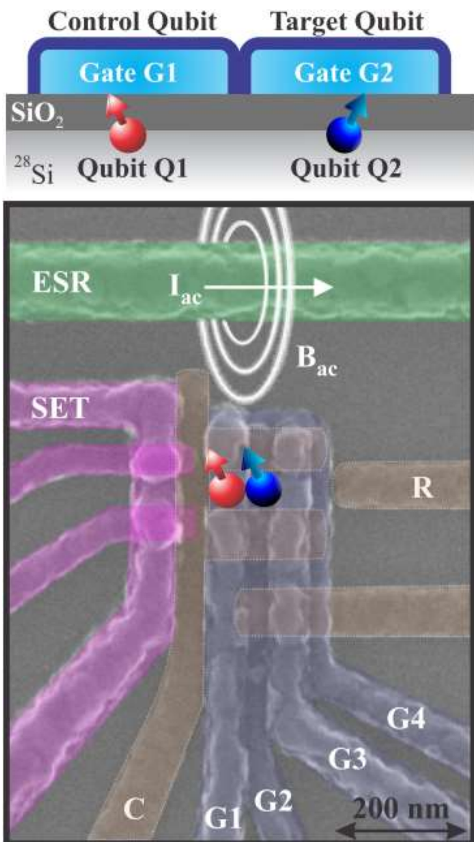
Dynamic Neuromorphic Asynchronous Processor Scalable-Learning (DynapSEL)

Tape out 11/16 – silicon expected 07/17

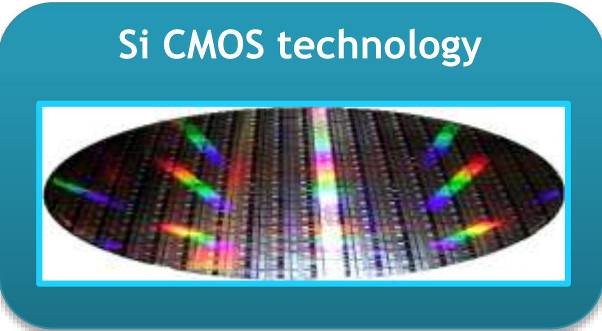


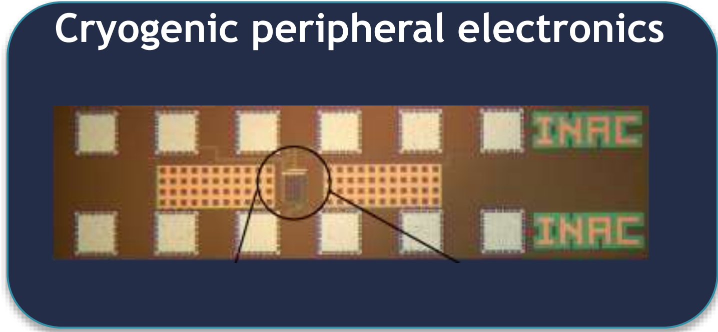
Chip Name	DynapSEL
Process	ST28FDSOI
Supply Voltage	1V
IO Number	176 + (internal 59)
Chip area	2.8mm x 2.6mm
Core Numbers	4 non-plastic cores 1 plastic core
Neuron Type	Analog AExp I&F
Non-plastic Synapse Type	TCAM based 4-bit
Plastic Synapse Type	Linear 4-bit digital
Throughput of Router	1G Events/second
Scalability	16 x16 chips non-plastic core) 4 x4 chips (plastic cores)

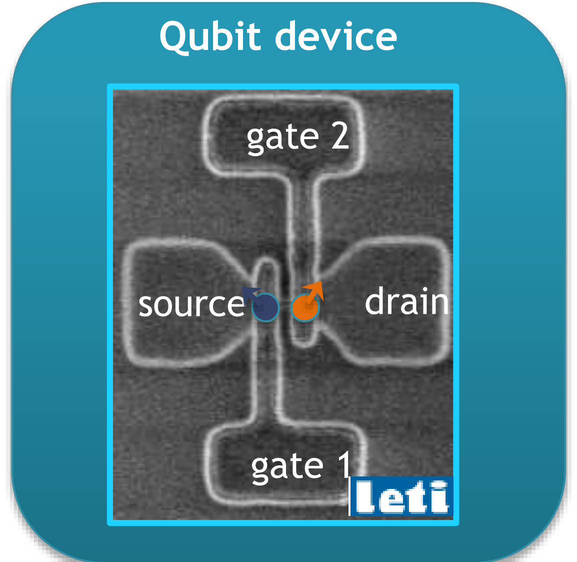
SI QUANTUM ELECTRONICS

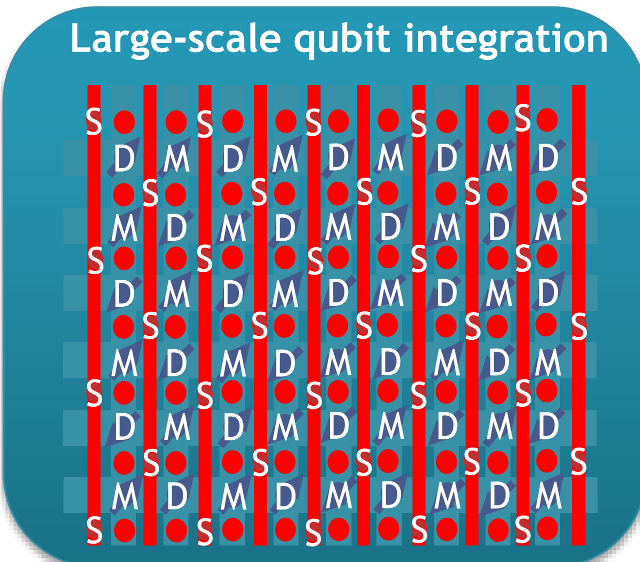


M. Veldhorst *et al.* (UNSW)
Nature 526, 410-414 (2015)

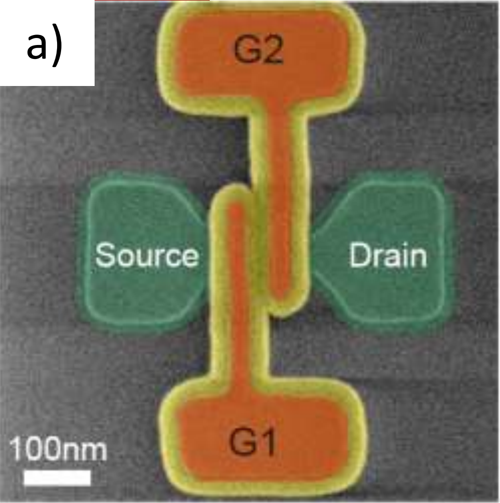


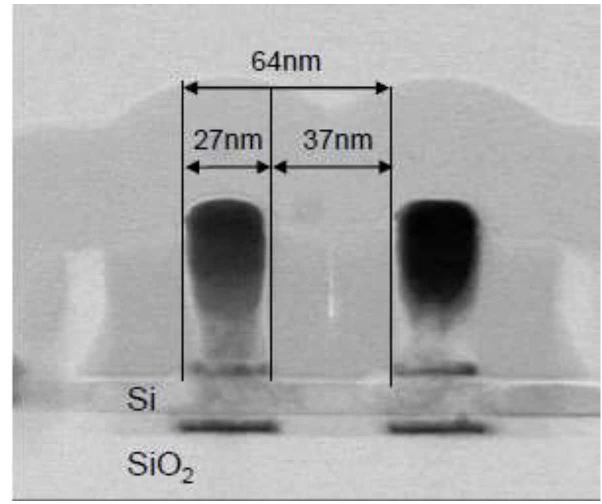


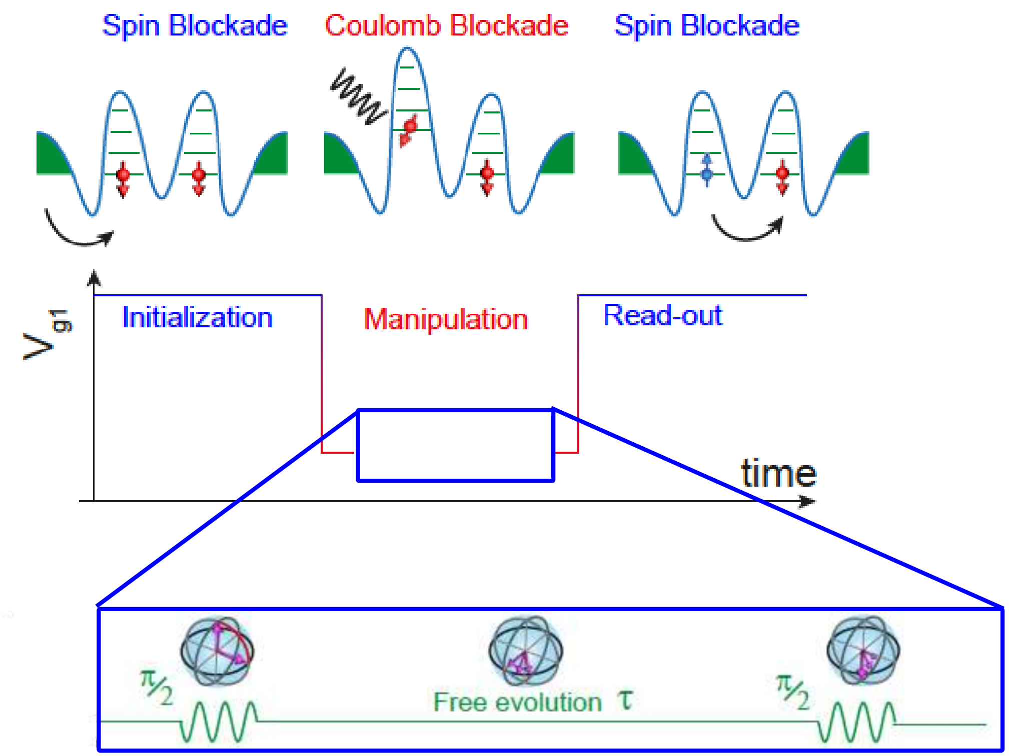


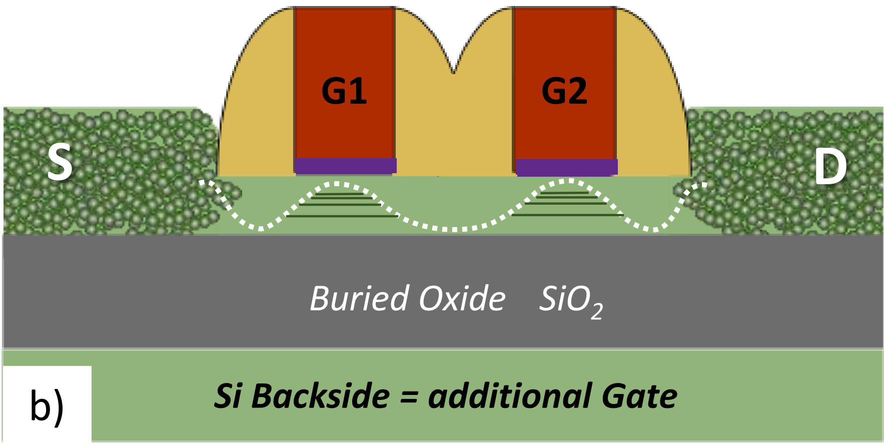


FIRST QBIT IN SI ON 300MM BASED ON FDSOI 28NM FLOW



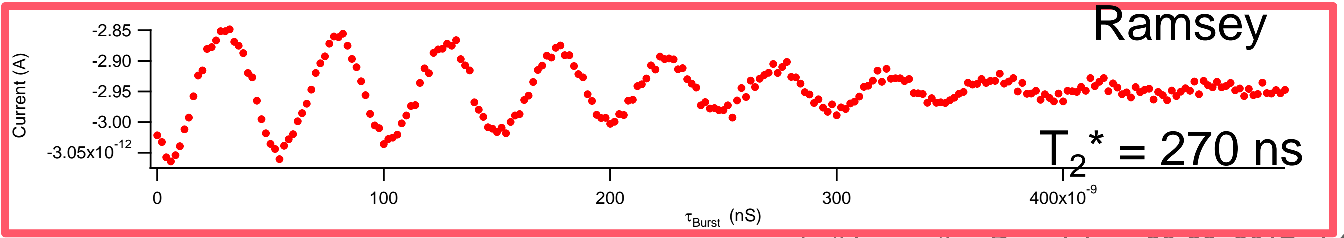






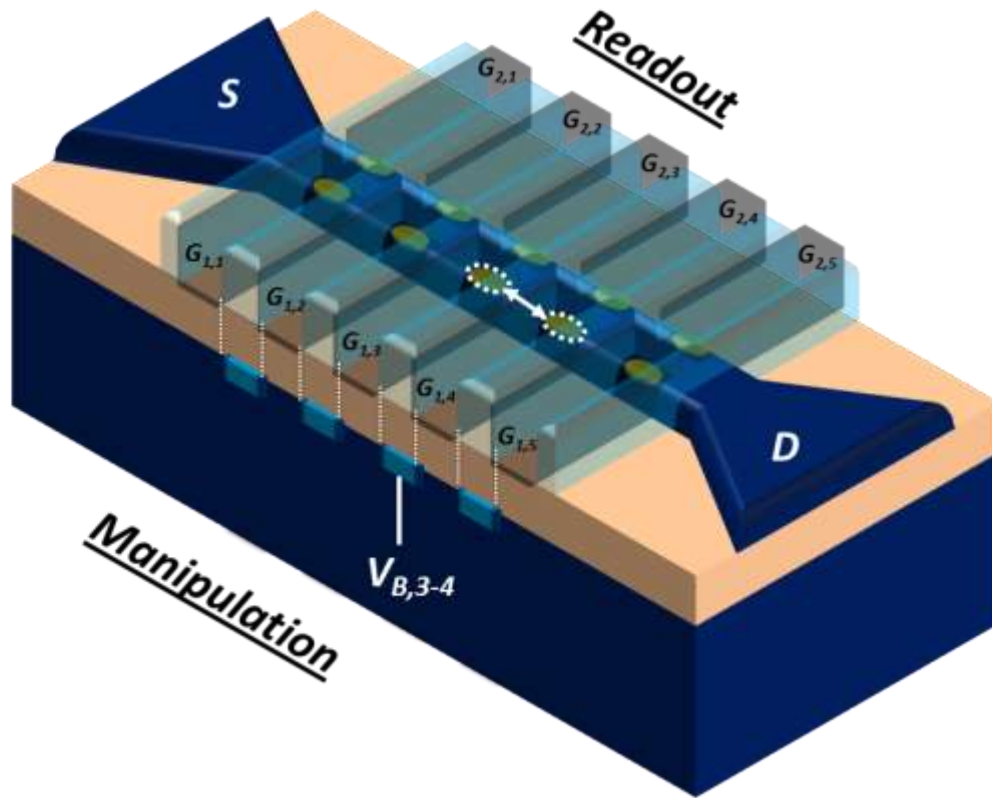
⇒ **Two QDs in series** coupled by tunnel junction

⇒ **Quantization** of the energy levels at low T



TOWARDS A REAL MULTI-QUANTUM BIT SYSTEM IN SI

Near-term:



- Pairs of **Split-Gates over a single Si NanoWire**
- **Spacing 40nm** or lower
- One side for data qubits, other side for **readout via reflectometry**
- **Tunable Nearest neighbor coupling** via (local) ground plane defined under the BOx

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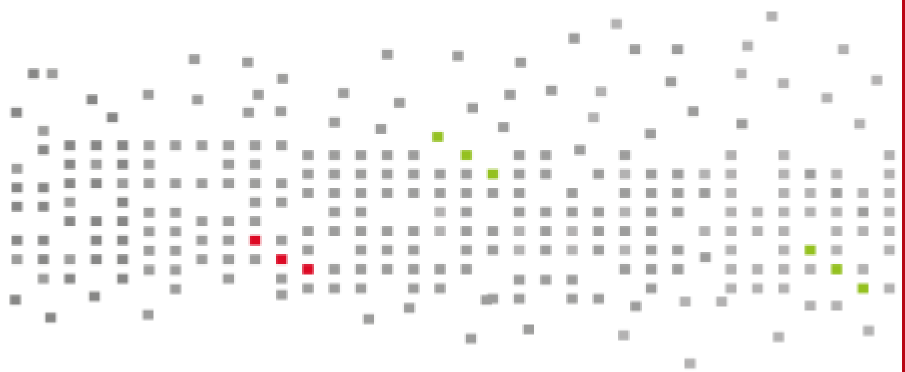
CONCLUSIONS

- **Time is short to show the work on materials that is also ongoing with Academia and tool suppliers but please come back and you will see the results**

- **LETI continue working on looking for new and disruptive ways to push forward computational power in the most efficient way**



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